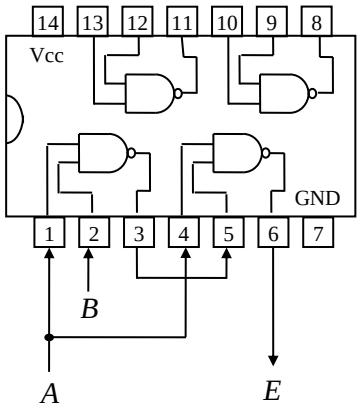
Remember to bring this along to your lab!

CS2100 Logic Trainer Guidelines

[This document is available on Canvas and course website https://www.comp.nus.edu.sg/~cs2100]

IMPORTANT NOTES

- You are to do the lab by yourself.
- Check the IC chips with the IC chip tester before you start the lab.
- Switch off the power while you are connecting your circuit.
- Place the IC chips in the correct orientation – the notch of the IC chip should be at the top.
- Align the pins of the chip with the holes on the breadboard properly before you press down the chip, or you may bend/break the pins.
- Make sure that the wire connections are neat to ease checking and debugging.
- Adopt a colour scheme for wires (e.g. green for inputs, blue for outputs, etc.). This is useful for debugging. The standard wire colours for power (Vcc) and ground (Gnd) are red and black respectively.
- Familiarize yourself with the logic probe and use it. Always attempt to debug yourself with the logic probe before asking your labTA for help. If you get excessive help, marks may be deducted.
- Once Once you have connected your circuit, get it accessed by your labTA before you dismantle your circuit. You may leave the room after your labTA has assessed your circuit and collected your lab report.
- Please complete everything and leave the room latest by 10 minutes before the end of the lab.
- Use the chip extractor to remove the IC chips from the breadboard and put all items back neatly into the tray before you leave the lab.
- Please prepare layout diagrams before the lab for your own use. See Figure 1. You need not hand in these diagrams if they are not asked for, but they are useful for wiring up your circuit, especially for complex ones.



Wiring for the expression

$E = ((A \cdot B)' \cdot A)'$

Figure 1.

- Please write and draw clearly and neatly. You may use pencil for logic diagrams. Untidy writing or drawing will be penalized. Some real students' samples are shown below.

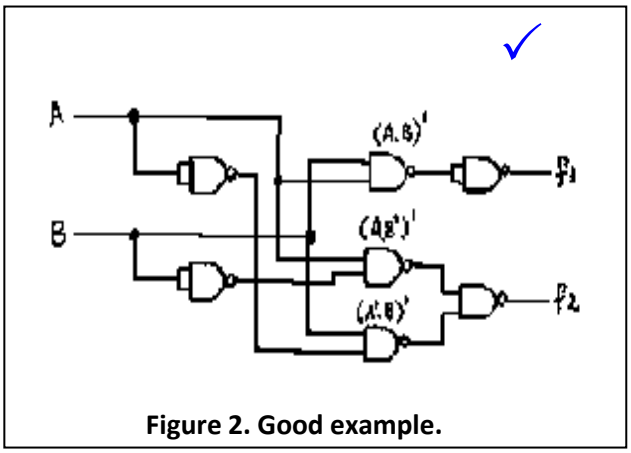


Figure 2. Good example.

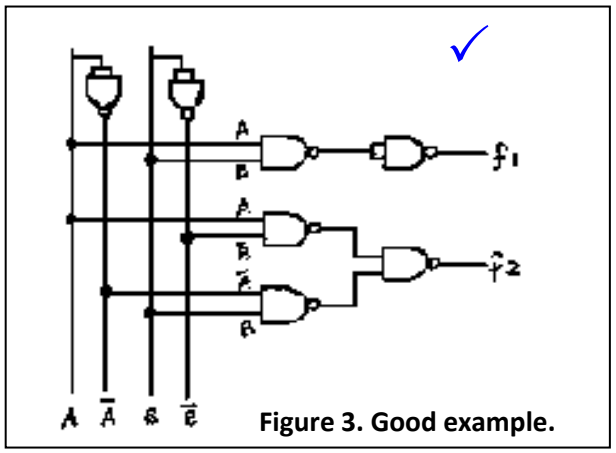


Figure 3. Good example.

Good: Lines are straights. All inputs and outputs are properly labelled.

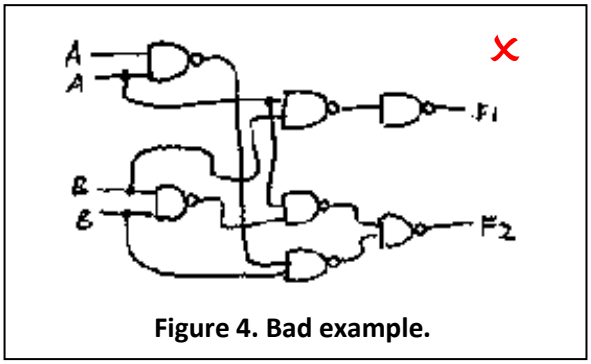


Figure 4. Bad example.

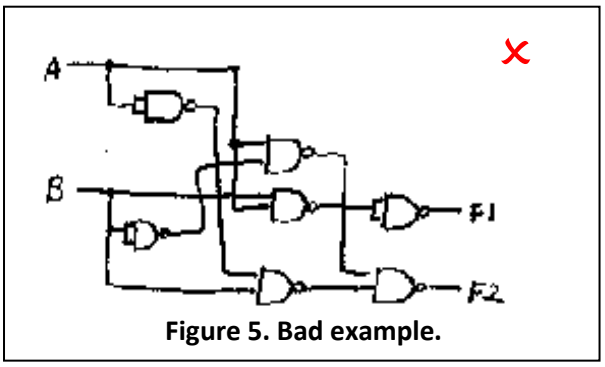


Figure 5. Bad example.

- When you are asked to draw **logic diagrams**, we are looking for diagrams that look like the one in Figure 6, not Figure 7, which shows the actual connection of the pins of the chip. The diagram in Figure 7 may be used for your own reference.

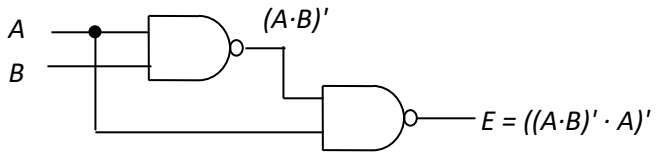


Figure 6. Logic diagram.

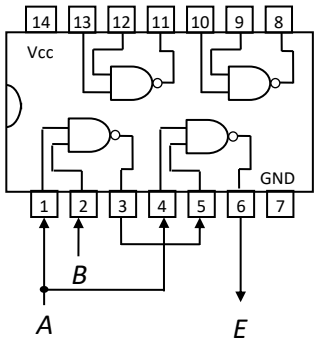


Figure 7. Pin connections.

- For logic diagrams, all lines should be straight. All inputs, outputs and intermediate outputs should be labelled, as shown in Figure 8. Use large black dot to indicate a fork.

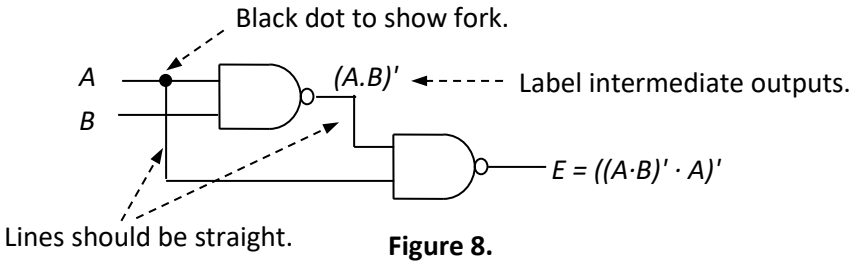


Figure 8.

- All inputs of a gate must be fed with some value. You should not leave any input unconnected. For example, to use a 2-input NAND gate as an inverter, here are two correct methods:

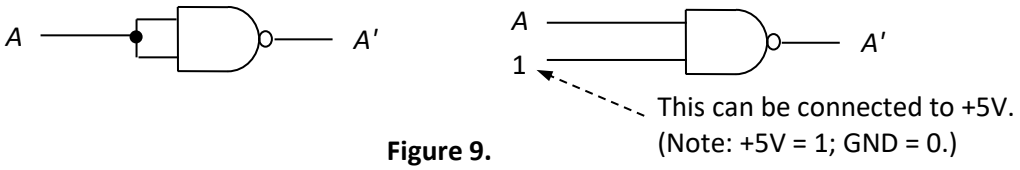


Figure 9.

- The following is wrong, even though it may appear to work on the logic trainer:

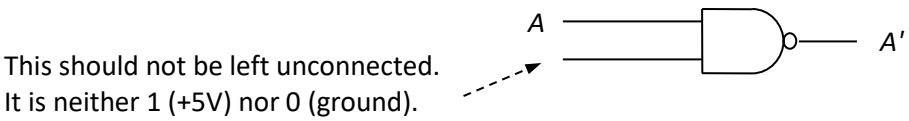


Figure 10.

- A logic gate has only one output. However, in subsequent labs, some devices may have multiple outputs. If you are not using all the outputs of the device, it is fine to leave the unused output unconnected.

Prepared by: Aaron Tan