CS2100 Computer Organisation

Tutorial #8: MSI Components

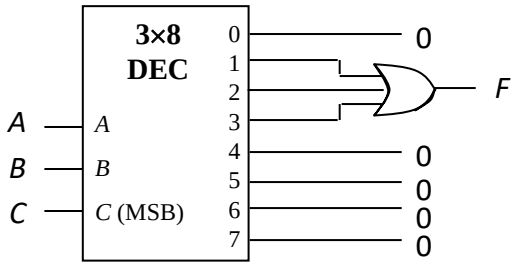
(Week 10: 24 – 28 March 2025)

Discussion Questions:

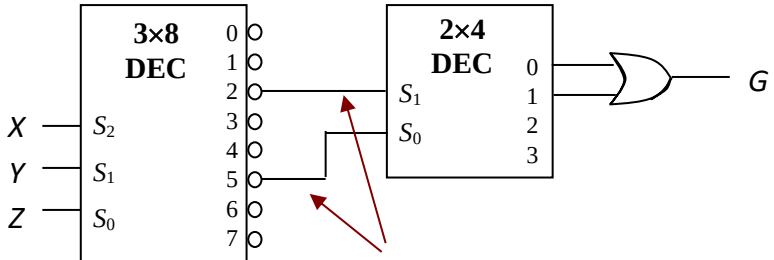
D1. Given this Boolean function:

$$F(A,B,C) = \Sigma\, m(1, 2, 3)$$

We want to implement this function using a **3×8 decoder with normal outputs** as shown below. Point out the mistakes in the solution below.

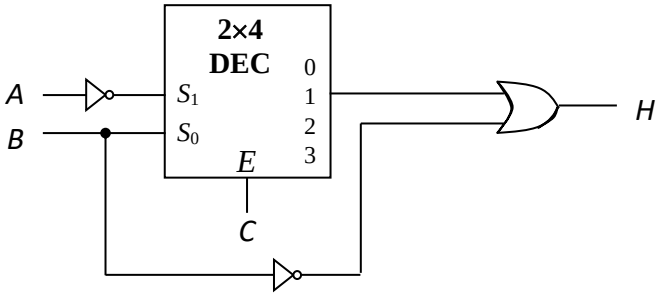


D2. Given the following circuit comprising a **3×8 decoder with negated outputs** and a **2×4 decoder with normal outputs**, what is the Boolean function *G*(*X,Y,Z*)?



How would you label these two intermediate outputs? (Use minterm or maxterm notation.)

D3. Given the following circuit comprising a **one-enabled 2×4 decoder with normal outputs**, what is the simplified SOP expression of Boolean function *H(A,B,C)*?



Tutorial Questions:

(Make sure you have done the above discussion questions.)

1. Realize the following function with (a) **an 8:1 multiplexer**, and (b) **a 4:1 multiplexer** using the first 2 input variables as the selector inputs.

   $$F(X, Y, Z) = \Pi M(1, 5, 6) \cdot D(4)$$

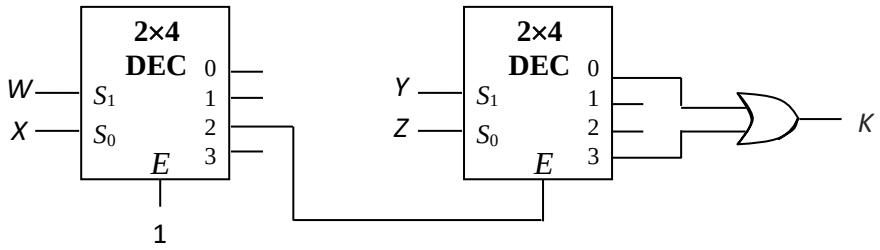
   You may write complemented variables instead of drawing an inverter to derive it. If you have several choices for your answer, choose the simplest one (constant logic values 0 and 1 are simpler than literals). You may write "x" or "d" for "don't-care" values.

   What if we use the last 2 input variables as the selector inputs instead for the 4:1 multiplexer?

2. You are given the following Boolean function: $K(W,X,Y,Z) = \Sigma m(8, 11)$.

   You are to implement this function using the fewest number of one-enabled 2×4 decoder with normal outputs and at most one logic gate? (Logic gates, as you have learned, are NOT, AND, OR, NAND, NOR, XOR, and XNOR.)

   The following is one solution. Is there a simpler circuit using just one decoder and one logic gate?



3. [AY2011/2 Semester 2 Exam question]
   You are to design a converter that takes in 4-bit input *ABCD* and generates a 3-bit output *FGH* as shown in Table 1 below.

Table 1

Input				Output		
A	***B***	***C***	***D***	***F***	***G***	***H***
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

Table 2

S	$Y_3Y_2Y_1Y_0$
0	$J_3J_2J_1J_0$
1	$K_3K_2K_1K_0$

You are given the following components:

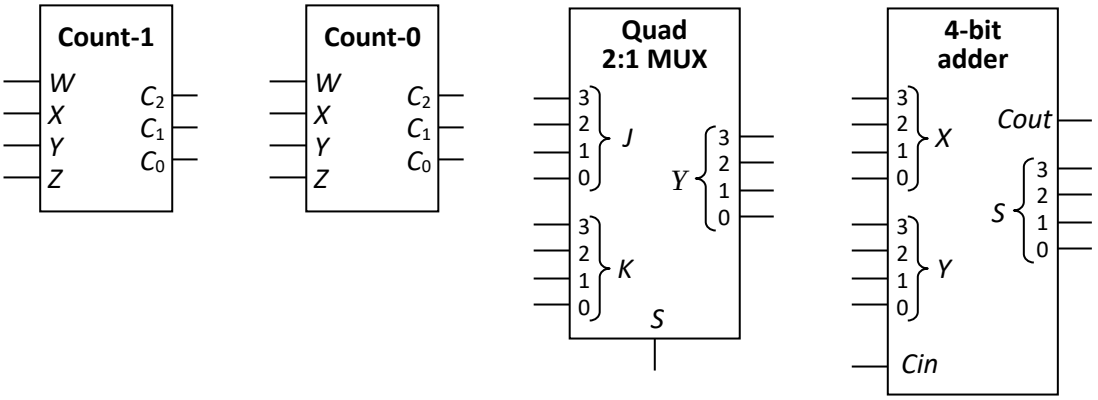
a. A **Count-1** device that takes in a 4-bit input *WXYZ* and generates a 3-bit output $C_2C_1C_0$ which is the number of 1s in the input. For example, if *WXYZ* = 0111, then $C_2C_1C_0$ = 011 (or 3).

b. A **Count-0** device that takes in a 4-bit input *WXYZ* and generates a 3-bit output $C_2C_1C_0$ which is the number of 0s in the input. For example, if *WXYZ* = 0111, then $C_2C_1C_0$ = 001 (or 1).

c. A **quad 2:1 multiplexer** that takes in two 4-bit inputs $J_3J_2J_1J_0$ and $K_3K_2K_1K_0$, and directs one of the inputs to its output $Y_3Y_2Y_1Y_0$ depending on its control signal *S*, as shown in Table 2 above.

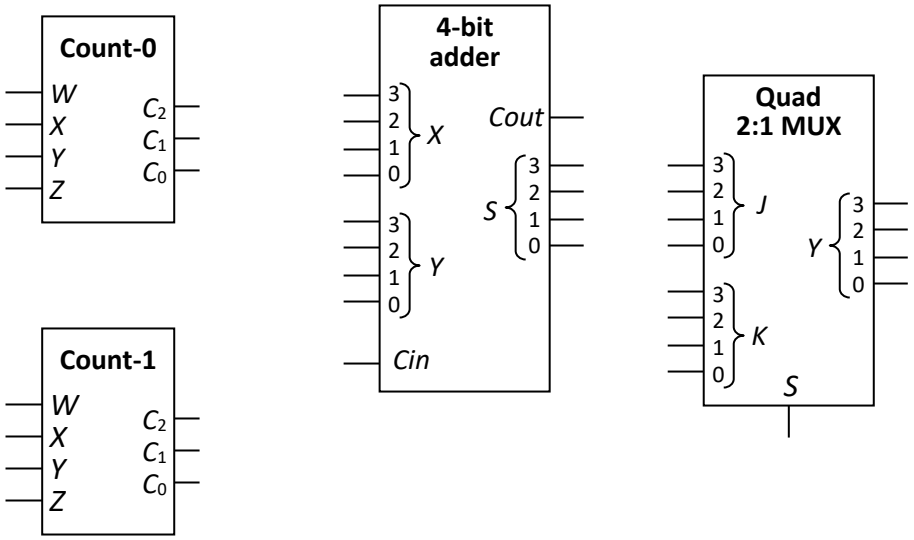
d. A **4-bit parallel adder** that takes in two 4-bit unsigned binary numbers and outputs the sum.

The block diagrams of these components are shown below:

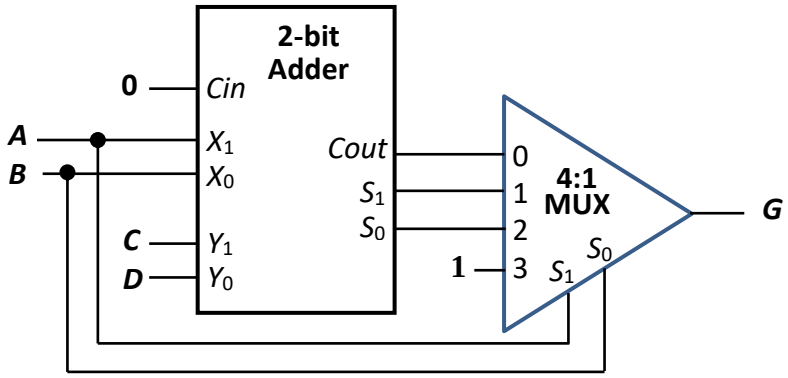


Given the above 4 components, you are to employ block-level design to design the converter, without using any additional logic gate or other devices. You may observe that if *A* = 1, then the output *FGH* is simply the number of 1s in the input *ABCD*. You are to make your own observation for the case when *A* = 0.

[Hint (not given in exam): You need only use one of each of the components. Complete the diagram below.]



4. [AY2024/25 Semester 1 Exam]
The circuit on the left below comprises a 2-bit parallel adder and a 4:1 multiplexer. Fill in the table on the right. Each entry in the table is a simplified SOP expression for $G(A, B, C, D)$.

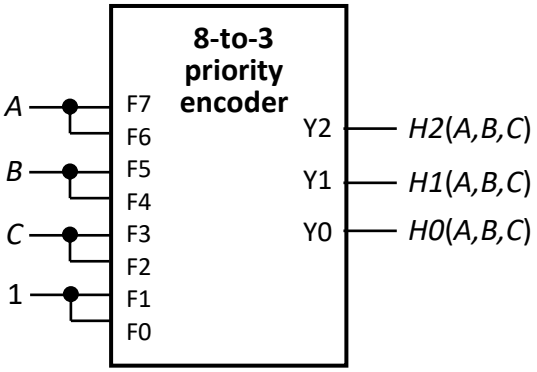


A	B	G(A,B,C,D)
0	0	
0	1	
1	0	
1	1	

Common mistake made in the exam: Many students wrote these answers for the second and third rows, which are wrong. Why?

A	B	G(A,B,C,D)
0	1	A'·B·C'·D + A'·B·C·D'
1	0	A·B'·D

5. [AY2024/25 Semester 1 Exam]
The circuit below uses an 8-3 priority encoder whose function is described in the table. What are the simplified SOP expressions for $H2(A, B, C)$, $H1(A, B, C)$ and $H0(A, B, C)$?



F7	F6	F5	F4	F3	F2	F1	F0	Y2	Y1	Y0
0	0	0	0	0	0	0	0	X	X	X
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1